

256 Bit Commercial X2210 64 x 4 Bit
 Industrial X2210I

Nonvolatile Static RAM

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FEATURES

- Single 5V Supply
- Fully TTL Compatible
- Infinite E²PROM Array Recall, RAM Read and Write Cycles
- Access Time of 300 ns Max.
- Nonvolatile Store Inhibit: $V_{CC} = 3V$ Typical
- High Reliability
 - Store Cycles: 100,000
 - Data Retention: 100 Years
- JEDEC Standard 18-Pin Package

DESCRIPTION

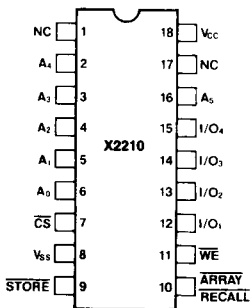
The Xicor X2210 is a 64 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2210 is fabricated with the same reliable N-channel floating gate MOS technology used

in all Xicor 5V nonvolatile memories. The X2210 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μ s.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 100,000 store cycles and inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION

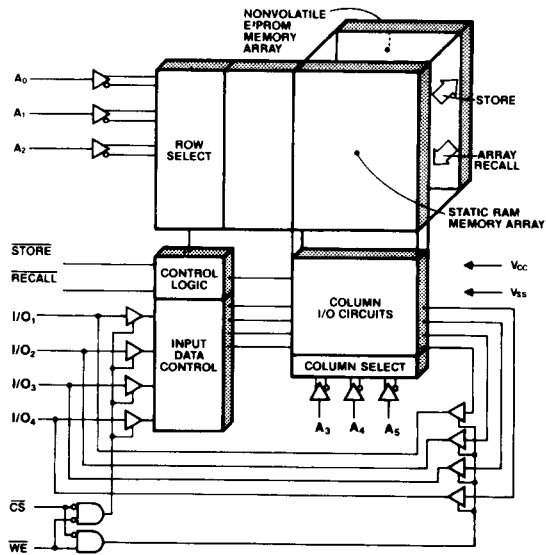


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PIN NAMES

| | |
|------------------------------------|---------------------|
| A ₀ -A ₅ | Address Inputs |
| I/O ₁ -I/O ₄ | Data Inputs/Outputs |
| WE | Write Enable |
| CS | Chip Select |
| ARRAY RECALL | Array Recall |
| STORE | Store |
| V _{CC} | +5V |
| V _{SS} | Ground |
| NC | No Connect |

FUNCTIONAL DIAGRAM



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X2210, X2210I

ABSOLUTE MAXIMUM RATINGS*

| | |
|-------------------------|-----------------|
| Temperature Under Bias | |
| X2210 | -10°C to +85°C |
| X2210I | -65°C to +135°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on any Pin with | |
| Respect to Ground | -1.0V to +7V |
| D.C. Output Current | 5 mA |
| Lead Temperature | |
| (Soldering, 10 Seconds) | 300°C |

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2210 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.

X2210I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.

| Symbol | Parameter | X2210 Limits | | X2210I Limits | | Units | Test Conditions |
|----------------|------------------------|--------------|----------------|---------------|----------------|---------------|---|
| | | Min. | Max. | Min. | Max. | | |
| I_{CC} | Power Supply Current | | 50 | | 55 | mA | All Inputs = V_{CC} $I_{I/O} = 0$ mA |
| I_{LI} | Input Load Current | | 10 | | 10 | μA | $V_{IN} = \text{GND to } V_{CC}$ |
| I_{LO} | Output Leakage Current | | 10 | | 10 | μA | $V_{OUT} = \text{GND to } V_{CC}$ |
| $V_{IL}^{(2)}$ | Input Low Voltage | -1.0 | 0.8 | -1.0 | 0.8 | V | |
| $V_{IH}^{(2)}$ | Input High Voltage | 2.0 | $V_{CC} + 1.0$ | 2.0 | $V_{CC} + 1.0$ | V | |
| V_{OL} | Output Low Voltage | | 0.4 | | 0.4 | V | $I_{OL} = 4.2$ mA |
| V_{OH} | Output High Voltage | 2.4 | | 2.4 | | V | $I_{OH} = -2$ mA |

ENDURANCE AND DATA RETENTION

| Parameter | Min. | Units | Conditions |
|----------------|---------|----------------------|---|
| Endurance | 10,000 | Data Changes Per Bit | Xicor Reliability Reports RR-520 and RR-504 |
| Store Cycles | 100,000 | Store Cycles | Xicor Reliability Reports RR-520 and RR-504 |
| Data Retention | 100 | Years | Xicor Reliability Report RR-515 |

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz, $V_{CC} = 5\text{V}$

| Symbol | Test | Max. | Units | Conditions |
|-----------------|--------------------------|------|-------|-----------------------|
| $C_{I/O}^{(1)}$ | Input/Output Capacitance | 8 | pF | $V_{I/O} = 0\text{V}$ |
| $C_{IN}^{(1)}$ | Input Capacitance | 6 | pF | $V_{IN} = 0\text{V}$ |

Notes: (1) This parameter is periodically sampled and not 100% tested.

(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

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A.C. CONDITIONS OF TEST

| | |
|--------------------------------|-------------------------------|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | 1 TTL Gate and $C_L = 100$ pF |

MODE SELECTION

| | | Inputs | | Input Output I/O | Mode |
|----|----|--------------|-------|------------------|------------------------------------|
| CS | WE | ARRAY RECALL | STORE | | |
| H | X | H | H | Output High Z | Not Selected ⁽³⁾ |
| L | H | H | H | Output Data | Read RAM |
| L | L | H | H | Input Data High | Write "1" RAM |
| L | L | H | H | Input Data Low | Write "0" RAM |
| X | H | L | H | Output High Z | Array Recall |
| H | X | L | H | Output High Z | Array Recall |
| X | H | H | L | Output High Z | Nonvolatile Storing ⁽⁴⁾ |
| H | X | H | L | Output High Z | Nonvolatile Storing ⁽⁴⁾ |

A.C. CHARACTERISTICS

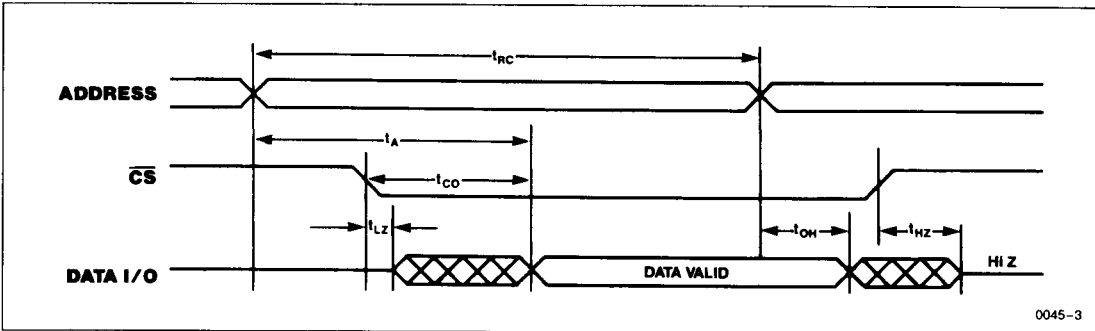
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X2210I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|----------------|-----------------------------------|------|------|-------|
| t_{RC} | Read Cycle Time | 300 | | ns |
| t_A | Access Time | | 300 | ns |
| t_{CO} | Chip Select to Output Valid | | 200 | ns |
| t_{OH} | Output Hold from Address Change | 50 | | ns |
| $t_{LZ}^{(5)}$ | Chip Select to Output in Low Z | 10 | | ns |
| $t_{HZ}^{(5)}$ | Chip Deselect to Output in High Z | 10 | 100 | ns |

Read Cycle



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Notes: (3) Chip is deselected but may be automatically completing a store cycle.

(4) STORE = L is required only to initiate the store cycle, after which the store cycle will be automatically completed (STORE = X).

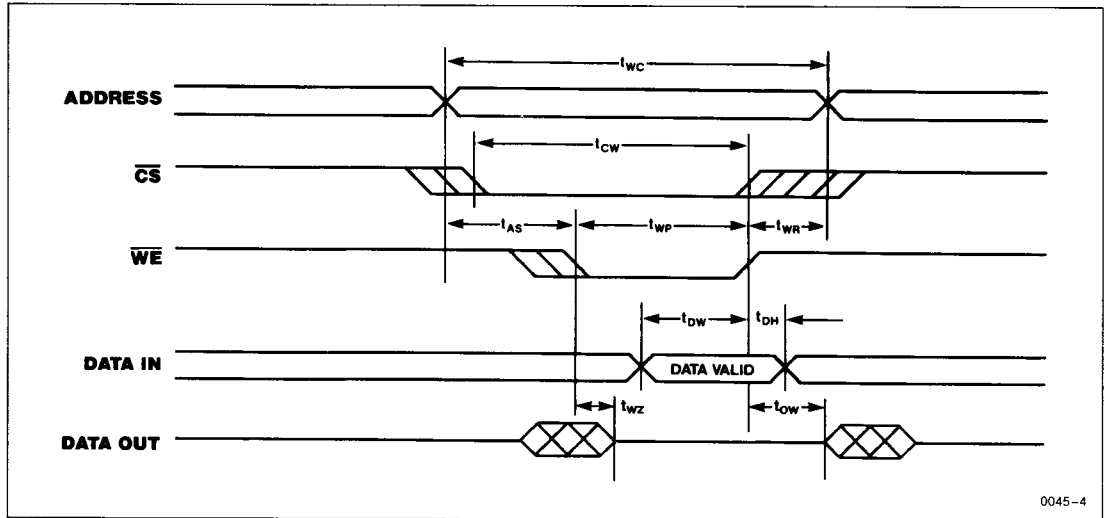
(5) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

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Write Cycle Limits

| Symbol | Parameter | | Min. | Max. | Units |
|----------|----------------------------------|--------|------|------|-------|
| t_{WC} | Write Cycle Time | | 300 | | ns |
| t_{CW} | Chip Select to End of Write | | 150 | | ns |
| t_{AS} | Address Setup Time | | 50 | | ns |
| t_{WP} | Write Pulse Width | | 150 | | ns |
| t_{WR} | Write Recovery Time | | 25 | | ns |
| t_{Dw} | Data Valid to End of Write | | 100 | | ns |
| t_{DH} | Data Hold Time | X2210 | 0 | | ns |
| | | X2210I | 20 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 10 | 100 | ns |
| t_{OW} | Output Active from End of Write | | 10 | | ns |

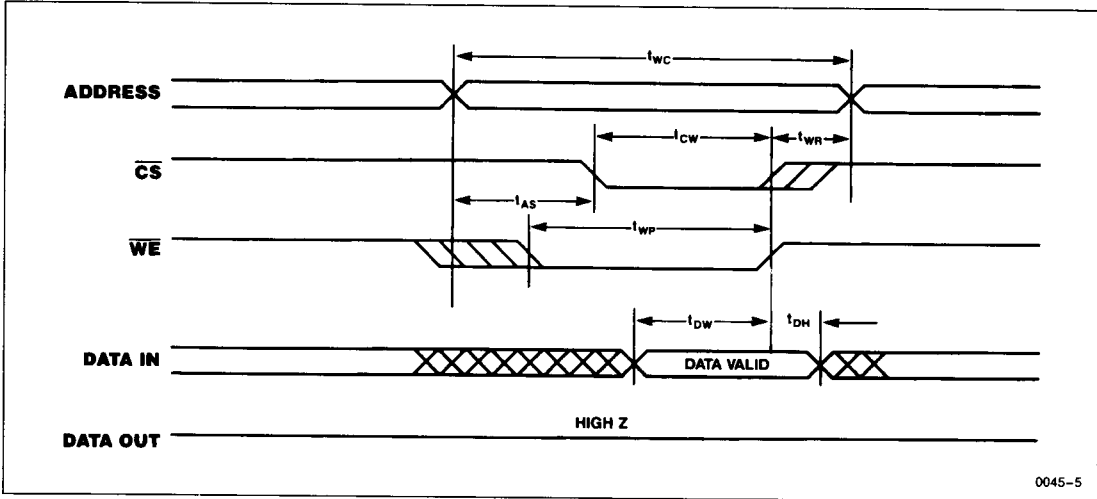
Write Cycle



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Early Write Cycle

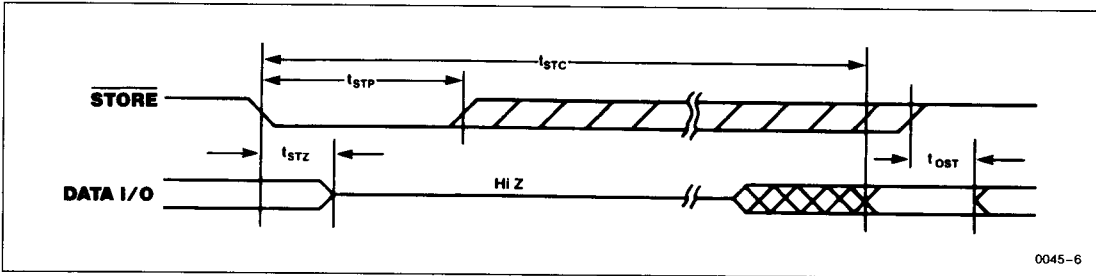


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Store Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|-----------|---------------------------------|------|------|-------|
| t_{STC} | Store Time | | 10 | ms |
| t_{STP} | Store Pulse Width | 100 | | ns |
| t_{STZ} | Store to Output in High Z | | 500 | ns |
| t_{OST} | Output Active from End of Store | 10 | | ns |

Store Cycle



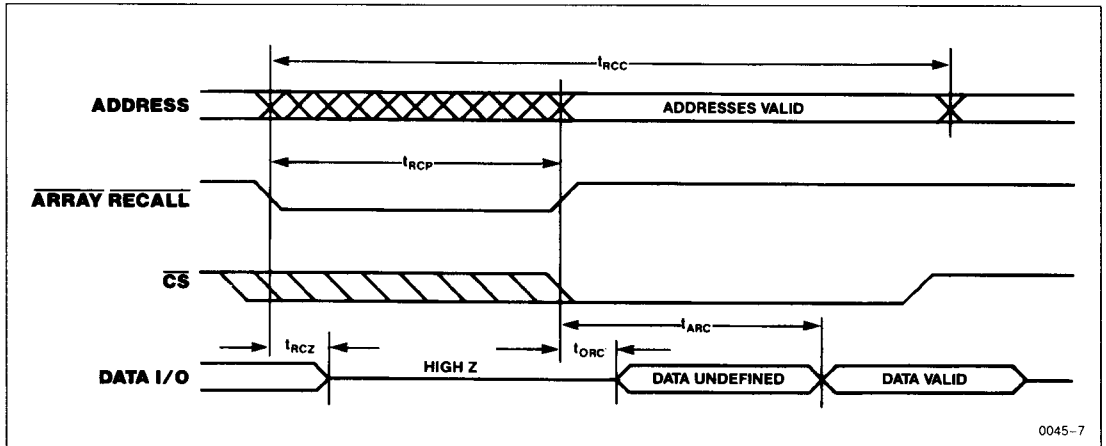
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Array Recall Cycle Limits

| Symbol | Parameter | Min. | Max. | Units |
|-----------|--|------|------|-------|
| t_{RCC} | Array Recall Cycle Time | 1200 | | ns |
| t_{RCP} | Recall Pulse Width ⁽⁶⁾ | 450 | | ns |
| t_{RCZ} | Recall to Output in High Z | | 150 | ns |
| t_{ORC} | Output Active from End of Recall | 10 | | ns |
| t_{ARC} | Recalled Data Access Time from End of Recall | | 750 | ns |

Array Recall Cycle



Note: (6) Array Recall rise time must be less than 1 μ s.

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PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A₀–A₅)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select (\overline{CS})

The Chip Select input must be LOW to enable read/write operations with the RAM array. \overline{CS} HIGH will place the I/O pins in the high impedance state.

Write Enable (\overline{WE})

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. \overline{WE} HIGH enables a read and \overline{WE} LOW enables a write.

Data In/Data Out (I/O₁–I/O₄)

Data is written to or read from the X2210 through the I/O pins. The I/O pins are placed in the high impedance state when either \overline{CS} is HIGH or during either a store or recall operation.

STORE

The STORE input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The \overline{WE} and ARRAY RECALL inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If STORE is asserted during a read operation, the read will be discontinued. If STORE is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

ARRAY RECALL

The ARRAY RECALL input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μ s or less.

An array recall has priority over RAM read/write operations and will terminate both operations when ARRAY RECALL is asserted. ARRAY RECALL LOW will also inhibit the STORE input.

WRITE PROTECTION

The X2210 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq 3V$, typically.
- Write Inhibit—Holding either STORE HIGH or ARRAY RECALL LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained. It should be noted; whichever method is employed, all control inputs should be stable and the device deselected prior to release of the controlling protection signal.
- Noise Protection—A STORE pulse of less than 20 ns (typical) will *not* initiate a store cycle.

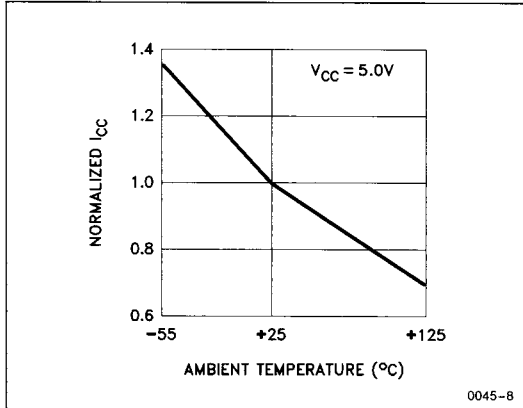
| Part Number | Store Cycles | Data Changes Per Bit |
|-----------------------|--------------|----------------------|
| X2210 X2210I | 10,000 | 1,000 |
| X2210/5 X2210I/5 | 50,000 | 5,000 |
| X2210/10 X2210I/10 | 100,000 | 10,000 |

SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|----------|------------------------------|-------------------------------|
| | Must be steady | Will be steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care : Changes Allowed | Changing : State Not Known |
| | N/A | Center Line is High Impedance |

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**Normalized Active Supply Current
vs. Ambient Temperature**



**Normalized Access Time
vs. Ambient Temperature**

